AMENDMENTS TO THE CLAIMS

Claims 1-59 (Cancelled)

60. (New) A semiconductor device comprising:

a semiconductor material having a surface and a first conductivity type;

a first region of the first conductivity type located in the semiconductor material, the first region contacting the surface;

a second region of a second conductivity type located in the semiconductor material, the second region contacting the surface and being spaced apart from the first region;

a third region of the first conductivity type located in the semiconductor material, the third region contacting the surface, being spaced apart from the first and second regions, and lying between the first and second regions, the third region being located such that no region of the second conductivity type lies between the first region and the third region;

a first polysilicon segment that contacts the surface and the first region;

a second polysilicon segment that contacts the surface and the second region, the second polysilicon segment being spaced apart from the first polysilicon segment; and

a third polysilicon segment that contacts the surface and the third region, the third polysilicon segment being spaced apart from the first and second polysilicon segments, and lying between the first and second polysilicon segments.

61. (New) The semiconductor device of claim 60 wherein the third polysilicon segment has a first portion and a second portion, and where the first portion is substantially higher than the second portion.

62. (New) The semiconductor device of claim 60 wherein a first portion of the third polysilicon segment vertically overlies and is isolated from the first polysilicon segment, and a second portion of the third polysilicon segment vertically overlies and is isolated from the second polysilicon segment.

63. (New) The semiconductor device of claim 61 wherein the semiconductor material has a dopant concentration, and the third region has a dopant concentration that is greater than the dopant concentration of the semiconductor material.

64. (New) The semiconductor device of claim 61 and further comprising:
a first layer of metal silicide located on the first polysilicon segment; and
a second layer of metal silicide located on the second polysilicon segment.

65. (New) The semiconductor device of claim 61 wherein the first polysilicon segment has the first conductivity type, the second polysilicon segment has the second conductivity type, and the third polysilicon segment has the first conductivity type.

66. (New) The semiconductor device of claim 60 wherein a portion of the first polysilicon segment and a portion of the second polysilicon segment lie vertically over the third polysilicon segment.

67. (New) The semiconductor device of claim 60 wherein the third polysilicon segment lies vertically under a portion of the first polysilicon segment and a portion of the second polysilicon segment.

68. (New) The semiconductor device of claim 66 wherein the semiconductor material has a dopant concentration, and the first region has a

dopant concentration that is greater than the dopant concentration of the semiconductor material.

69. (New) The semiconductor device of claim 66 and further comprising:

a first layer of metal silicide located on the first polysilicon segment; and

a second layer of metal silicide located on the second polysilicon segment.

70. (New) The semiconductor device of claim 66 wherein the first polysilicon segment has the first conductivity type, the second polysilicon segment has the second conductivity type, and the third polysilicon segment has the first conductivity type.

71. (New) A method of operating a semiconductor device, the semiconductor device comprising:

a semiconductor material having a surface and a first conductivity type;

a first region of the first conductivity type located in the semiconductor material, the first region contacting the surface;

a second region of a second conductivity type located in the semiconductor material, the second region contacting the surface and being spaced apart from the first region;

a third region of the first conductivity type located in the semiconductor material, the third region contacting the surface, being spaced apart from the first and second regions, and lying between the first and second regions, the third region being located such that no region of the second conductivity type lies between the first region and the third region;

a first polysilicon segment that contacts the surface and the first region;

a second polysilicon segment that contacts the surface and the second region, the second polysilicon segment being spaced apart from the first polysilicon segment;

a third polysilicon segment that contacts the surface and the third region, the third polysilicon segment being spaced apart from the first and second polysilicon segments, and lying between the first and second polysilicon segments;

a first layer of metal silicide located on the first polysilicon segment; and

a second layer of metal silicide located on the second polysilicon segment,

the method comprising the steps of:

applying a first voltage to the first layer of metal silicide; and

applying a second voltage to the second layer of metal silicide, the first and second voltages causing a reverse breakdown of a junction between the second region and the semiconductor material such that metal atoms from a layer of metal silicide migrate to form a metallic path through the junction.

72. (New) The method of claim 71 wherein the metallic path extends from the first poly silicon segment to the second polysilicon segment.